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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to market

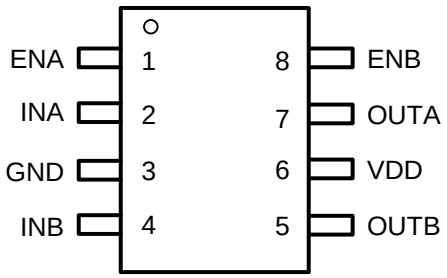
Revision 1.1: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT52240QSTDR	Tape & Reel	4000	2240Q	8	SOP-8L

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
ENA, ENB	-0.3	26	V
INA, INB	-5	26	V
OUTA, OUTB	-0.3	VDD+0.3	V
OUTA, OUTB (Pulse<0.2us)	-3	VDD+0.3	V
VDD	-0.3	26	V

Top View: SOP-8pin
Plastic



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V_{IN}=12V, T_A= 25°C.

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Figure 7. Input to Output Propagation Delay vs Temperature

Figure 8. ROH vs Temperature

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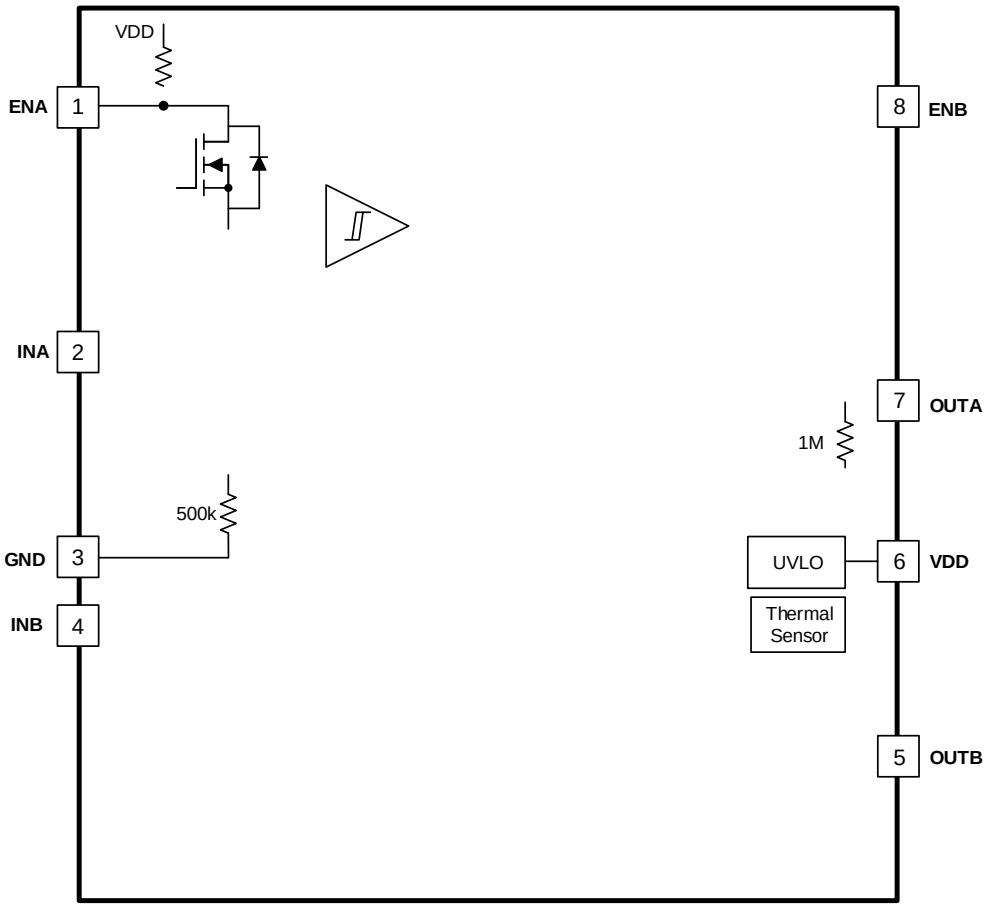

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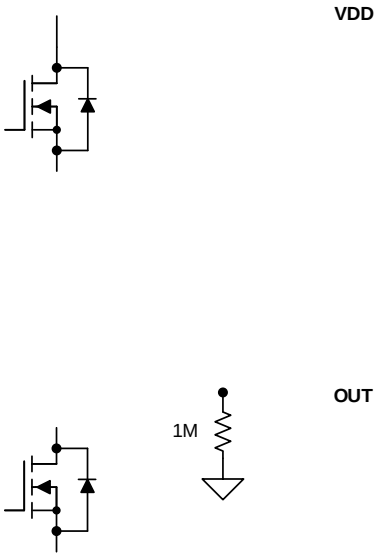

Figure 12. SCT52240Q Output Stage

Stackable Output

The SCT52240Q features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be stackable when the driven power device required higher driving capability. For example, in a Boost Power Factor Correction converter, there are 2 power MOSFET in parallel to support higher power output capability. The two power MOSFET are preferred to be driven by a common gate control signal. By using SCT52240Q, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA and INB. As a result, a single input signal controls the stacked output combination. To support the stackable output, each channel output stage artificially implements up to 5ns dead-time to avoid the possible shoot-through between two channels as shown Figure 13.

Due to the rising and falling threshold mismatch between INA and INB, cautions must be taken when implementing stackable output of OUTA and OUTB together. The maximum mismatch between INA and INB input threshold is up to 10mV (maximum cross temperature), as a result the allowed minimum slew rate of input logic signal is 2V/us. The following suggestions are recommended when INA and INB connected together and along with the OUTA and OUTB:

1. Apply the fast slew rate dv/dt on input (2 V/us or greater) to avoid the possible shoot-through between OUTA and OUTB output stage.
2. INA and INB must be connected as close to the pins as possible.

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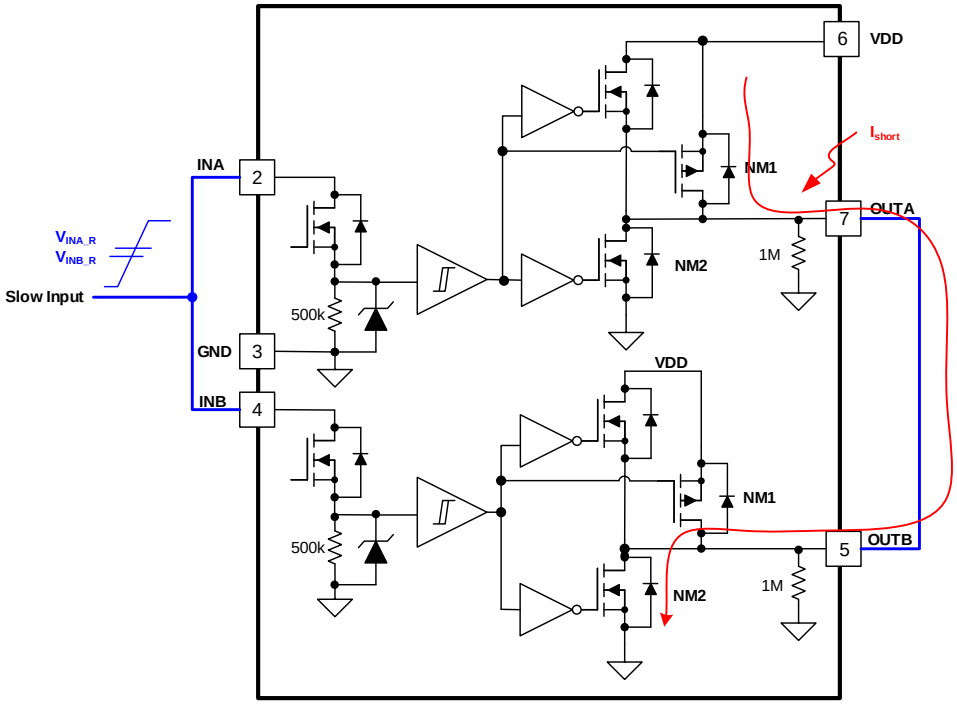

Figure 13. SCT52240Q Stackable output

The Figure 14 and Figure 15 shows the stackable output with 2V/us input signal.

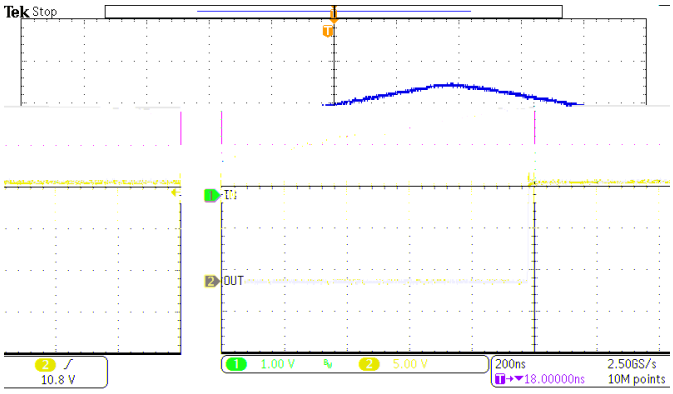

Figure 14. Driver Switching ON

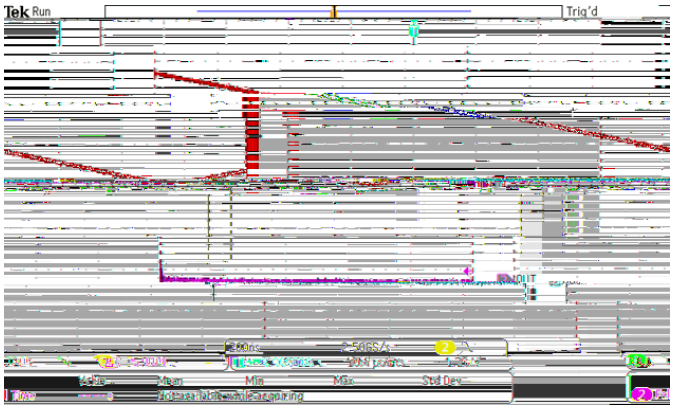

Figure 15. Driver Switching OFF

Thermal Shutdown

Once the junction temperature in the SCT52240Q exceeds 170 C, the thermal sensing circuit stops switching until the junction temperature falling below 145 C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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Typical Application

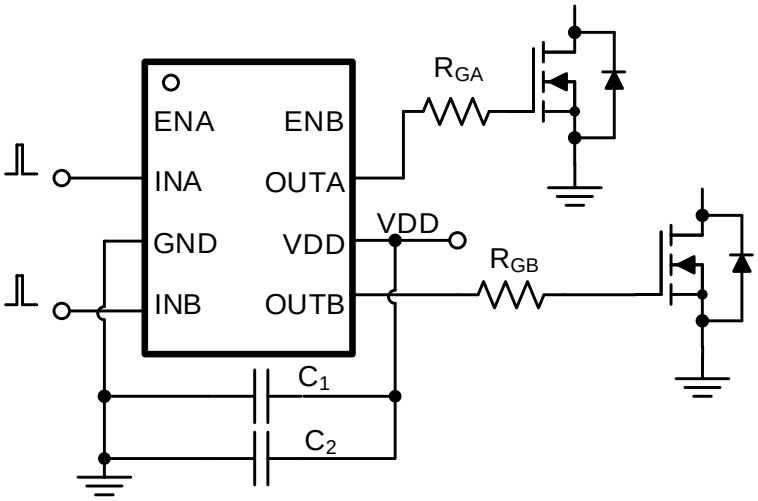

Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52240Q depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52240Q features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52240Q is:

(1)

Where

- V_{DD} is supply voltage
- C

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(3)

Where

- R_{OH} is the equivalent pull up resistance of SCT52240Q
- R_{OL} is the pull down resistance of SCT52240Q
- R_G is the gate resistance between driver output and gate of power device.

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Application Waveforms

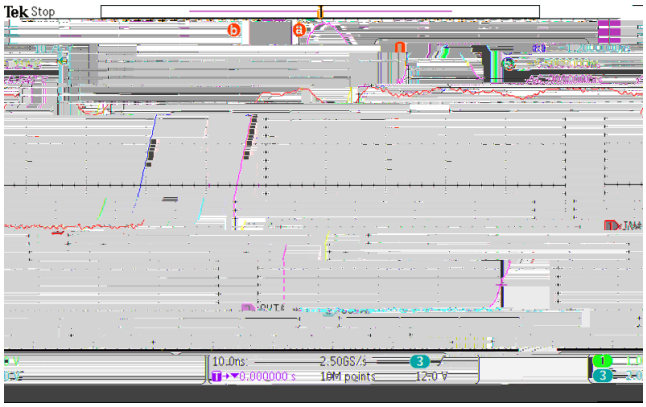

Figure 17. Driver Switching ON

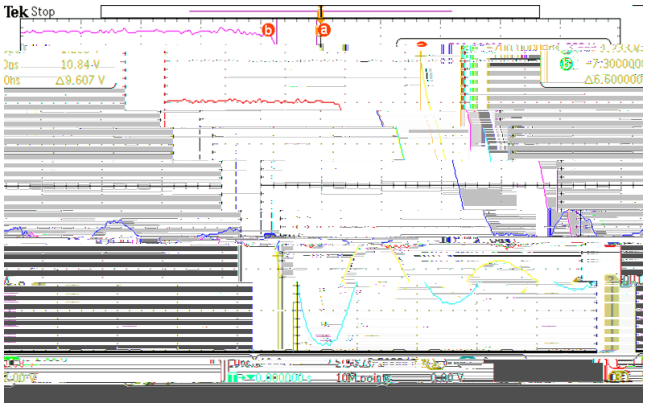

Figure 18. Driver Switching OFF

Figure 19. Delay Matching Rise

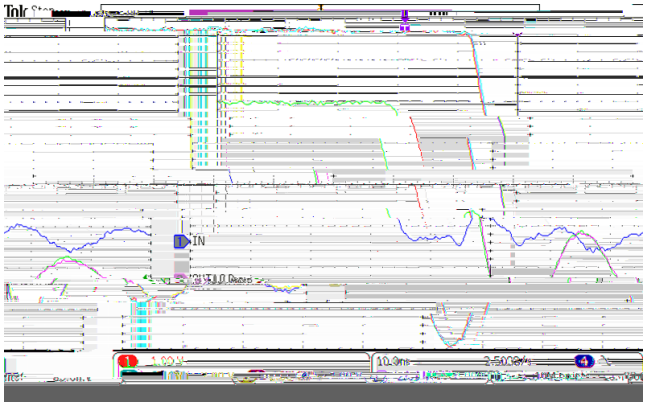

Figure 20. Delay Matching Fall

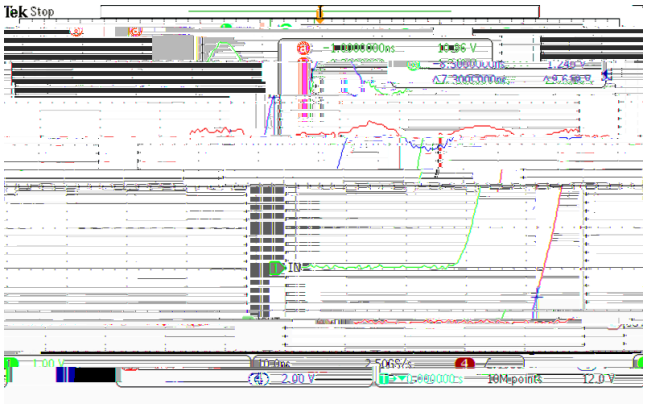

Figure 21. Stackable Output Rise

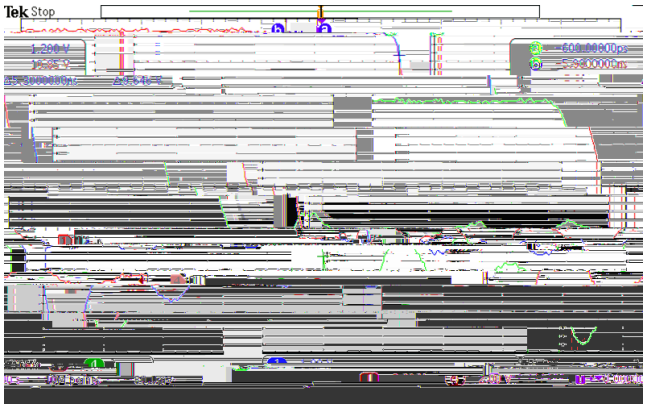

Figure 22. Stackable Output Fall

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Layout Guideline

The SCT52240Q provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. Below are the layout recommendations with using SCT52240Q and Figure 23 is the layout example.

Put the SCT52240Q as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD pin and GND pin to reduce the supply ripple. For the output stackable application, the driver input loop of two-channel input must be strictly symmetrical to ensure the input propagation delay is the same.

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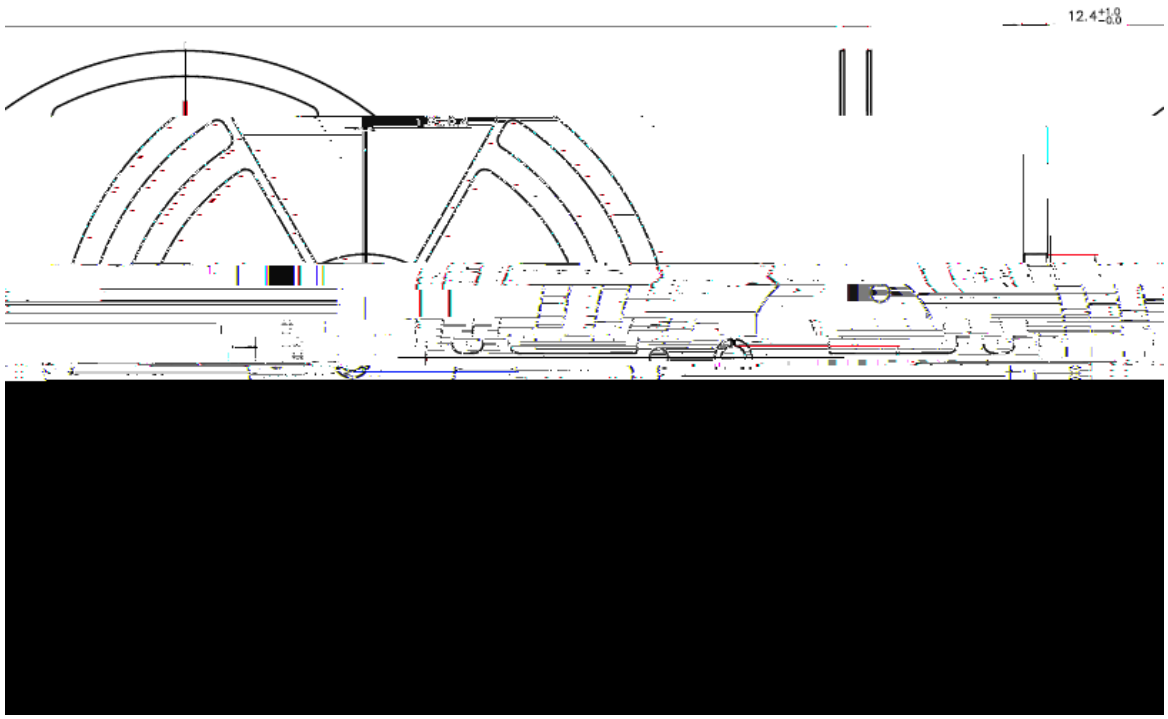

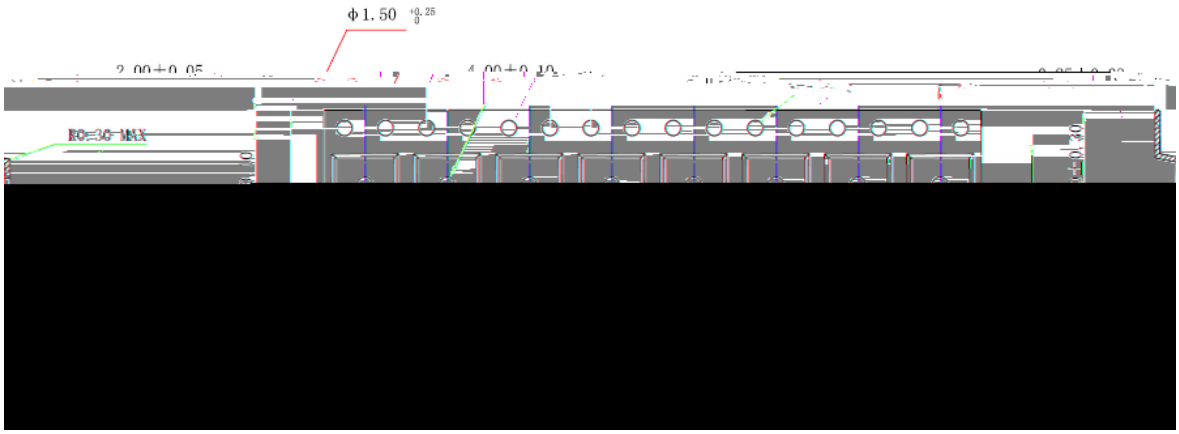

Feeding Direction